

8080 efficiently computes 32-by-16-bit quotient

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Occupying about half the space in memory as the routine proposed by Swift and Eisenstein¹, this program quickly performs a 32-bit-by-16-bit division. Also included with this tightened version is an efficient 16-bit-by-16-bit program of the type often used to multiply the result of a 32-bit-by-16-bit division by a third number.

The divider program is similar to Swift and Eisenstein's routine, subtracting the divisor from the most-significant 16 bits of the dividend. The appropriate bit of

the quotient is set or cleared, depending upon whether the subtraction process yields a 0 or 1 for that bit. The dividend is then shifted 1 bit with respect to the divisor, and the process is repeated. Sixteen such subtractions are necessary in order to generate the quotient and the remainder.

The dividend is stored in registers HL-DE, with the most significant digits in HL. The divisor is placed in register pair BC. The quotient will build up in DE, with the remainder in HL.

In the multiplication routine, the multiplicand is stored in BC, and the multiplier in HL. The result will appear in registers HL-DE. □

References

1. G. W. Swift and J. P. Eisenstein, "8080 program computes 32-by-16-bit quotient," *Electronics*, May 10, 1979, p. 143.

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay \$50 for each item published.

Tight. Shortened version of 32-by-16-bit divider routine retains all of the capabilities of the quotient program of Swift and Eisenstein¹, but occupies only half the space in memory. 16-by-16-bit multiplier program (opposite page, top) is a useful companion to the divider routine.

TABLE 1: 8080 PROGRAM: 32-BY-16 DIVISION

Label	T STATES	Source statement	Comments
DIV	4	MOV A, L	;
	4	SUB C	;
	4	MOV A, H	;
	4	SBB B	;
	6/2	RNC	; RETURN ON OVERFLOW
LOOP	4	XRA A	; INITIALIZE COUNTER
	10	DAD H	; SHIFT LEFT MUST SIG. PART OF DIVIDEND
	12	PUSH PSW	; SAVE COUNTER AND CARRY
	4	XCHG	; SHIFT LEFT
	10	DAD H	; LEAST SIG.
	4	XCHG	; PART OF DIVIDEND
	7/10	JNC L1	;
	6	INX H	; CONVEY CARRY IF THERE
	4	MOV A, L	; SUBTRACT
	4	SUB C	; DIVISOR
L1	4	MOV L, A	; FROM
	4	MOV A, H	; MOST SIG.
	4	SBB B	; 16 BIT
	4	MOV H, A	; OF DIVIDEND
	7/10	JC L2	; JUMP IF DIVISOR GREATER
	10	POP PSW	; UNSAVE COUNTER AND CARRY
	6	INX D	; APPEND '1' TO QUOTIENT
L3	10	JMP L4	;
L2	10	POP PSW	; UNSAVE COUNTER AND CARRY
	7/10	JC L3	;
L4	10	DAD B	; RESTORE DIVIDEND
	7	ADI 10H	; INCREMENT COUNTER
	7/10	JNC LOOP	; LOOP 16 TIMES
	10	RET	

TABLE 2: 8080 PROGRAM: 16-BY-16 MULTIPLICATION

Label	Source statement	Comments
MUL	XRA A	; INITIALIZE COUNTER
	MOV D, A	; INITIALIZE LEAST SIG
	MOV E, A	; PART OF PRODUCT
LOOP	DAD H	; SHIFT LEFT MULTIPLIER
	RAR	; SAVE CARRY
	XCHG	; SWAP FOR
	DAD H	; SHIFT LEFT PRODUCT
	JNC L1	
	INX D	; CONVEY CARRY IF THERE
L1	RAL	; UNSAVE CARRY
	JNC L2	; IF SET
	DAD B	; ADD IN MULTIPLICAND
	JNC L2	
	INX D	; CONVEY CARRY IF THERE
L2	XCHG	; SWAP BACK
	ADI 10H	; INCREMENT COUNTER
	JNC LOOP	; LOOP 16 TIMES
	RET	

Calculator notes

HP-97 speeds design of rf amplifiers

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Complementing the calculator note presented by Tula¹ for designing Class C tube-type amplifiers, this HP-97 program drastically reduces the time needed to build low-power radio-frequency amplifiers of the transistor variety. Given the large signal parameters and characteristics of the transistors used and the reactances of the

decoupling inductors and capacitors, the program quickly yields the values of the elements required in the amplifier's input and antenna-matching networks (for a one-stage amp) or the matching and interstage networks (for a two-stage design).

The program first finds the parallel-equivalent output resistance of one or both of the amplifiers from $R_p = (V_{cc} - V_{ce(sat)})^2 / 2P_o$, where V_{cc} is the specified collector voltage, P_o is the desired output power, and $V_{ce(sat)}$, the collector-to-emitter saturation voltage, is typically 2 volts. The loaded Q of the amplifier is then found from $Q_L = f_o / BW$, where f_o is the frequency of operation and BW is the bandwidth required.

Following this very simple calculation, the series-equivalent resistances and reactances are readily found

